wireless and wireline access systems, a backplane comprising:

aggregate traffic rates of up to approximately two gigabits per second comprises:

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for said low tier bus.

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gigabits per second.

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(New) The backplane as set forth in Claim 1 wherein said low tier that is capable of

a low tier bus comprising a switching architecture that (1) allows a circuit board card

on an input side of a connection to transmit data to a circuit-board card on an output side of said

(New) For use in association with devices such as processors and modems used in

a high tier that is capable of aggregate traffic rates of up to approximately twenty

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11. of aggregate t	(New) The backplane as set forth in Claim 10 wherein said high tier that is capable raffic rates of up to approximately twenty gigabits per second comprises: a high tier bus; and
	at least two switch matrix circuit board cards coupled to said high tier bus.
12.	(New) The backplane as set forth in Claim 11 wherein said high tier bus comprises: high speed serial links coupled to said at least two switch matrix circuit board cards
and coupled to circuit board cards capable of sending and receiving high speed data traffic.	
13. comprise:	(New) The backplane as set forth in Claim 12 wherein said high speed serial links
a receive path	point-to-point serial links comprising differential pairs for both a transmit path and
14. operate at a cl	(New) The backplane as set forth in Claim 13 wherein said high speed serial links ock rate equal to a clock rate of said backplane.
15. clock rate is 6	(New) The backplane as set forth in Claim 14 wherein said high speed serial link 5.536 MHz.
	(New) The backplane as set forth in Claim 14 comprising a high speed serial link l device that multiplies said high speed serial link clock rate by a factor of twenty (20), ach high speed serial link is 8B/10B encoded.
17. serial links for	(New) The backplane as set forth in Claim 12 comprising at least two (2) high speed each interface control processor slot in said backplane.
18. division multipetest bus.	(New) The backplane as set forth in Claim 1 further comprising one of: a time plex bus, a communications bus, a common control bus, and a Joint Test Access Group
19. clock and fran	(New) The backplane as set forth in Claim 18 further comprising at least one set of ning resources.

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